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MS-7505 ATX

Version: 20

CPU: Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe / Kentsfield family processors in LGA775 Package.

System Chipset:

NVIDIA MCP73

On Board Device:

BIOS -- SPI Flash 8M
Azalia Codec -- ALC888
LPC Super I/O -- FINTEK F71882FG
LAN -- Realtek RTL8211BL-GR
CLOCK Gen -- Integrated in MCP73
1394 Controller -- JMB381

Main Memory:

SINGLE-channel DDR-II * 4 (Max 4GB)

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 4

Intersil PWM

OPT	Function	Orcad Configure	BOM
PV	MCP73PV (HDMI+DVI) / F71882FG/ALC888/RTL8211BL/JMB381	cfg-7505-PV	601-7505-A10



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Size Custom

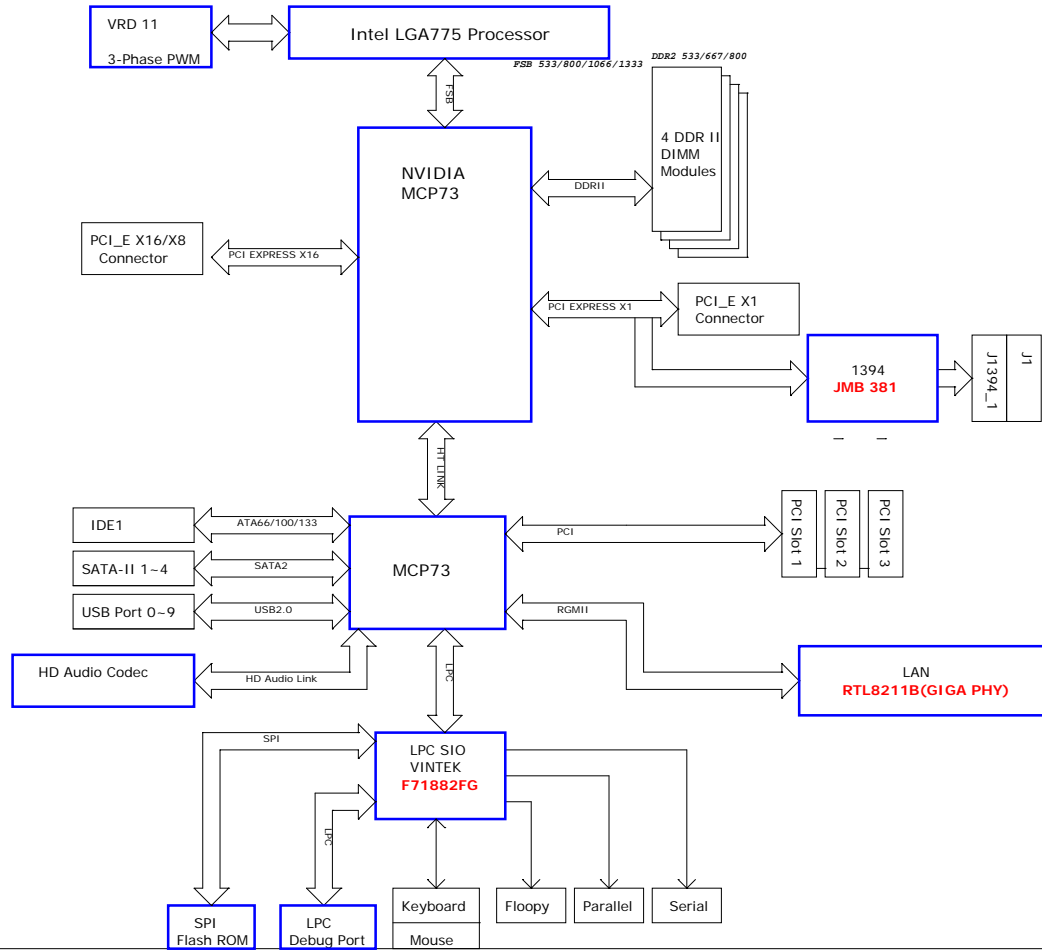
Document DescriptionCOVER SHEET

Rev DA

Date: Tuesday, February 15, 2006

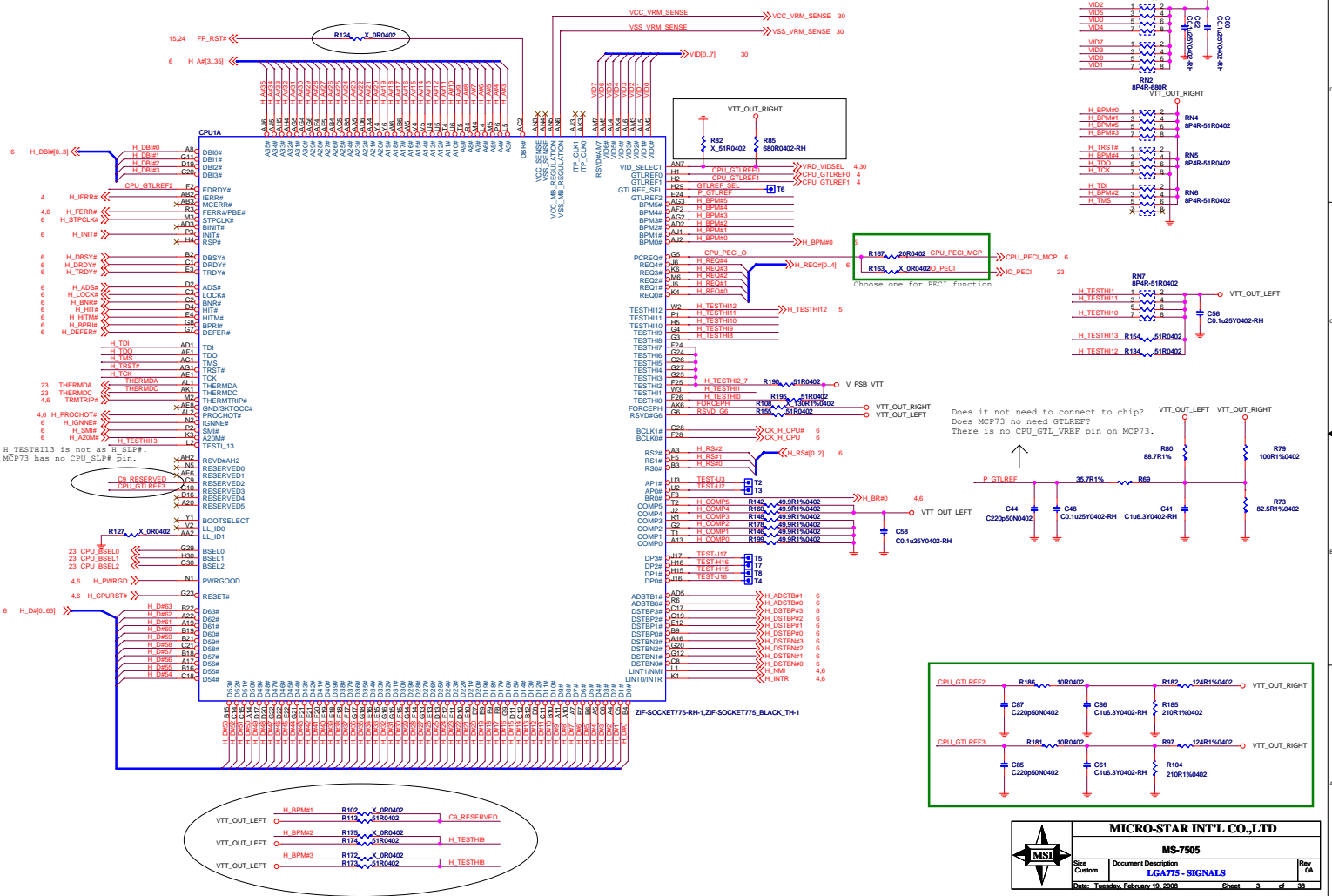
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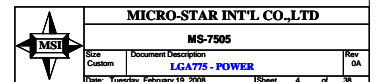
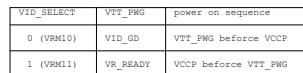
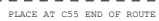
Block Diagram

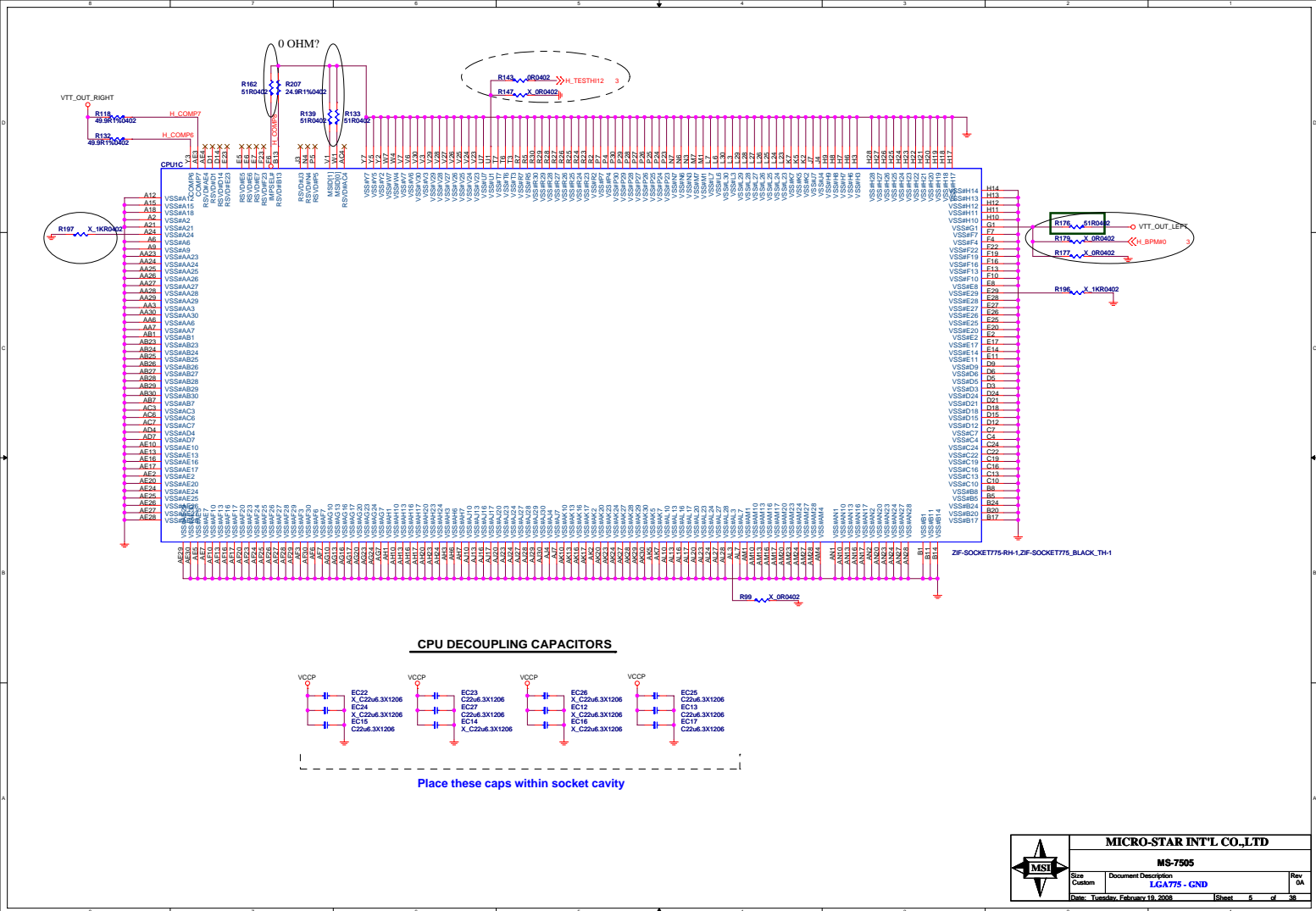


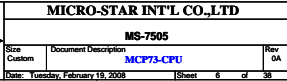
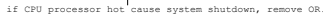
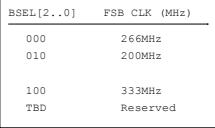
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MS-7505		
Doc Custom	Document Description BLOCK DIAGRAM	Rev 0A
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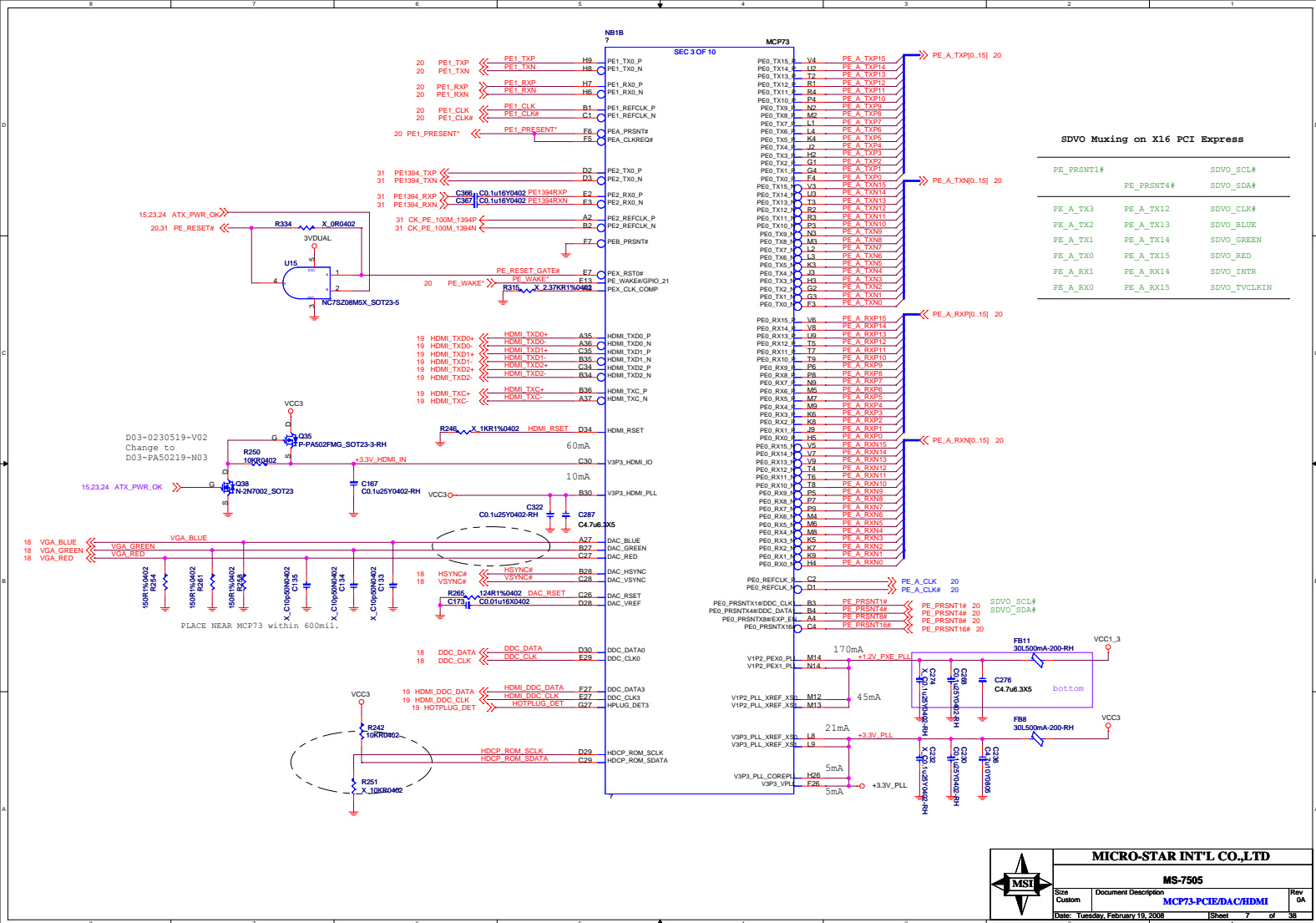
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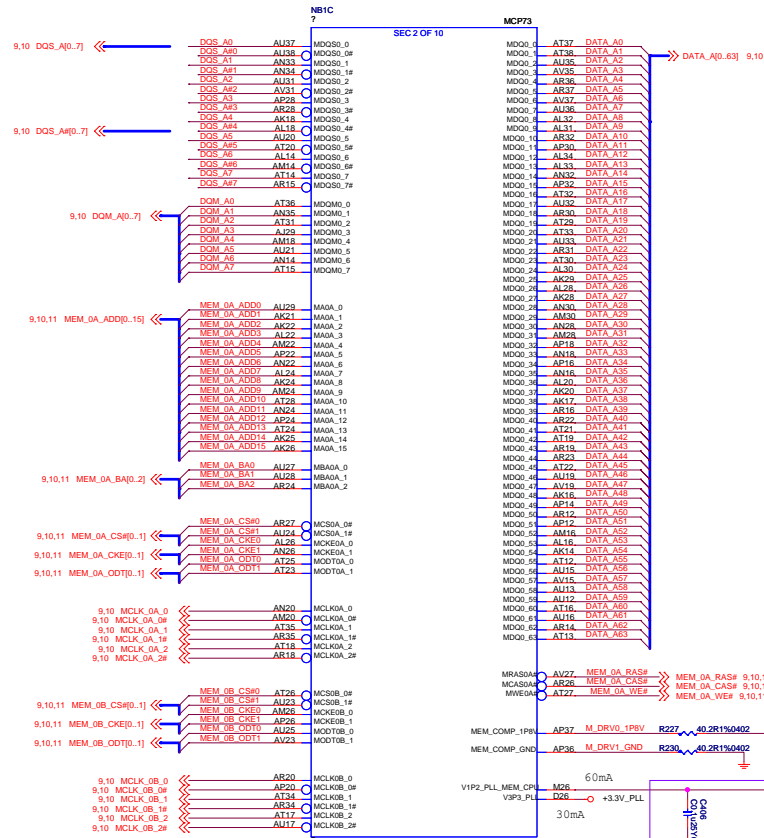










DIMM 0A

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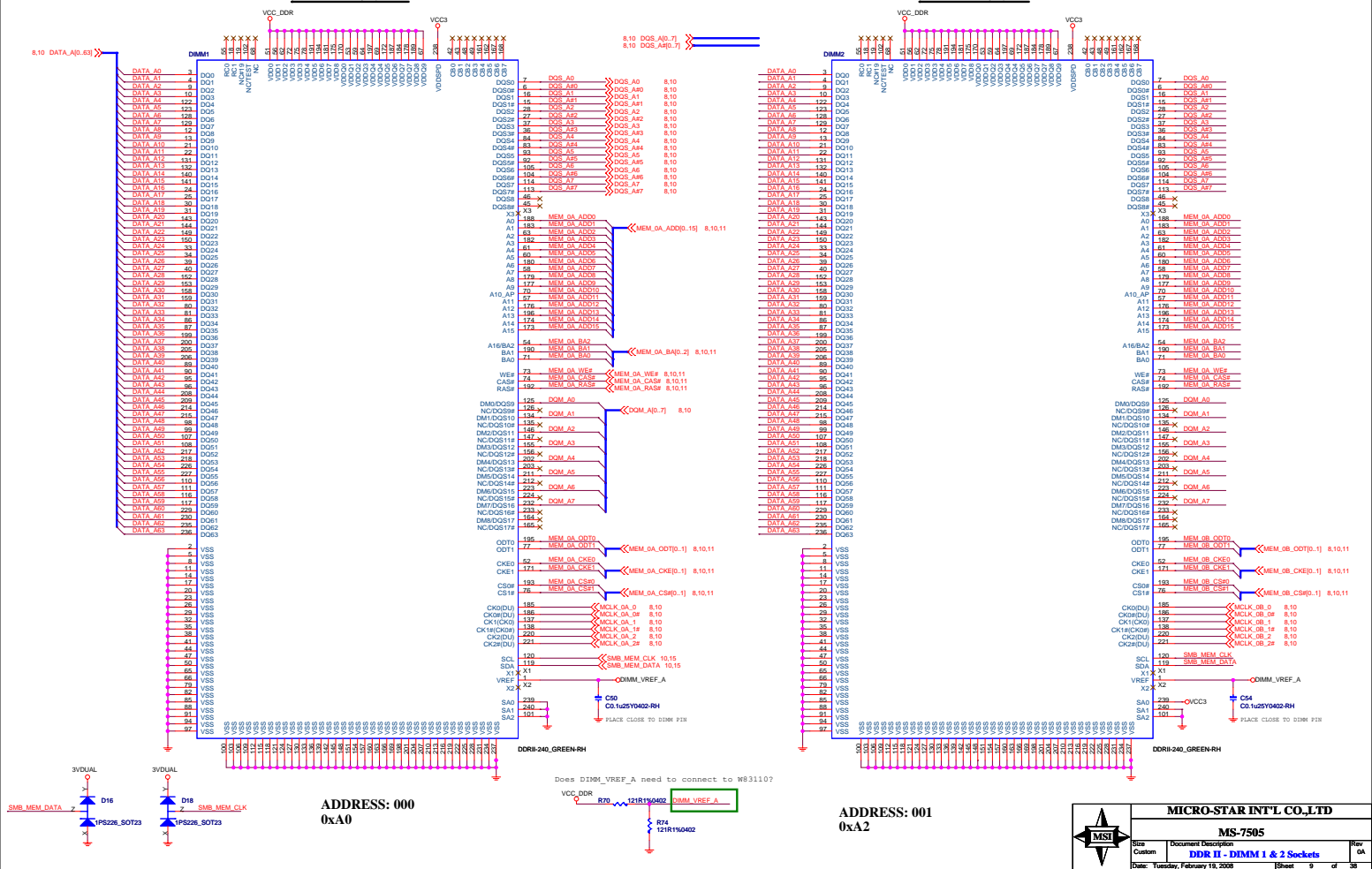
MS-7505

Size
Custom

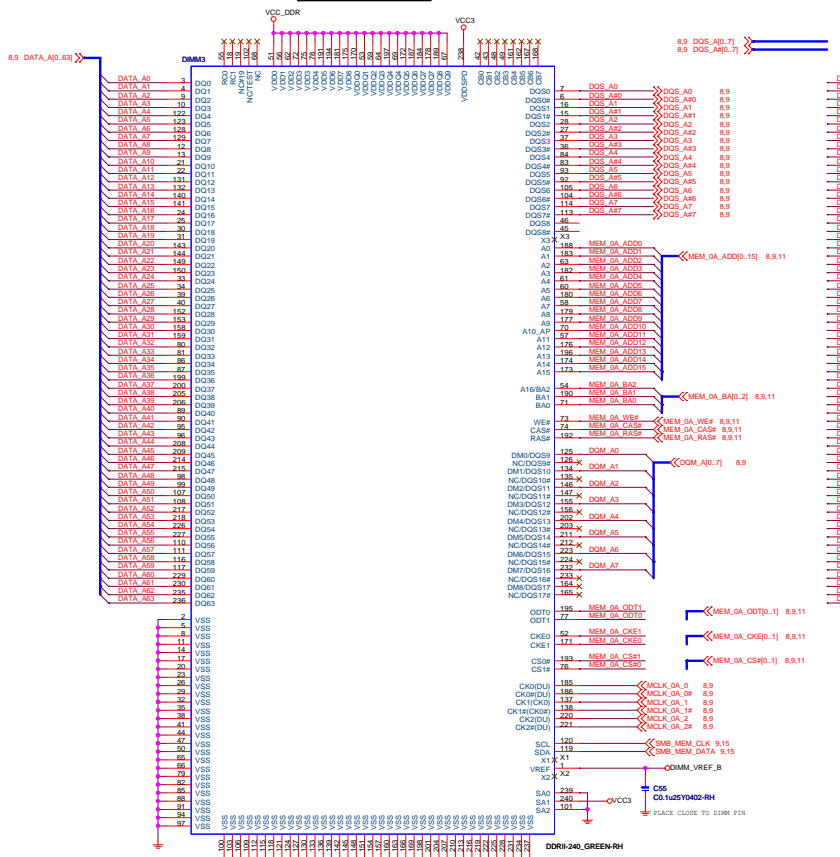
MCP73-MEM

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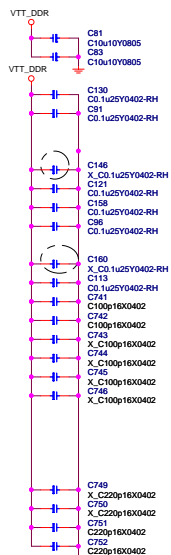
Rev
0A

DIMM2 / 0B

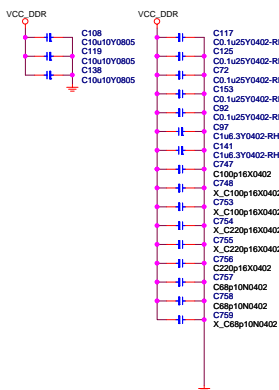
DIMM3



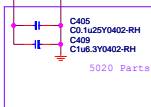
CHANNEL A VTT_DDR DECOUPLING CAPS

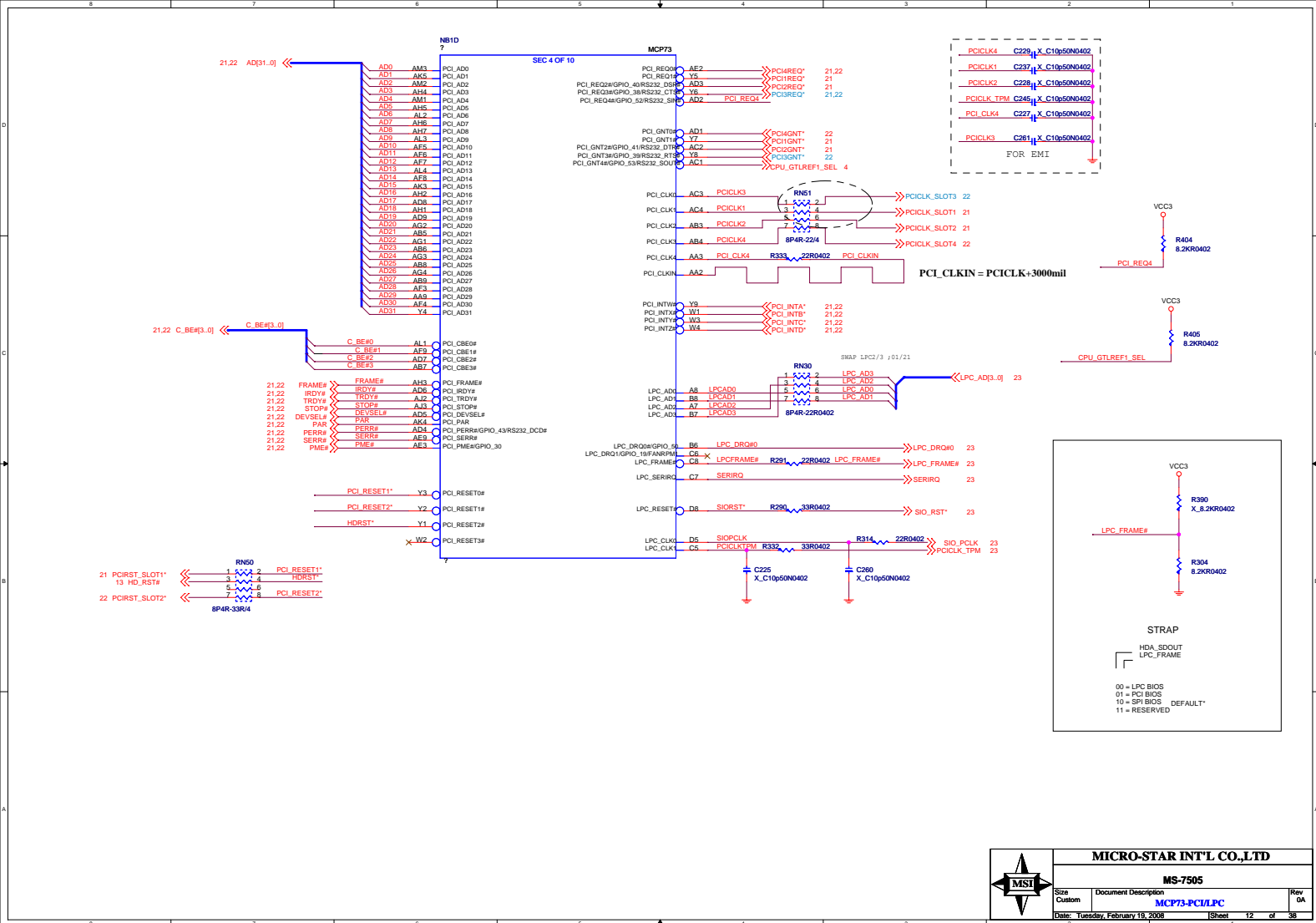


CHANNEL A ---- 0A , 0B

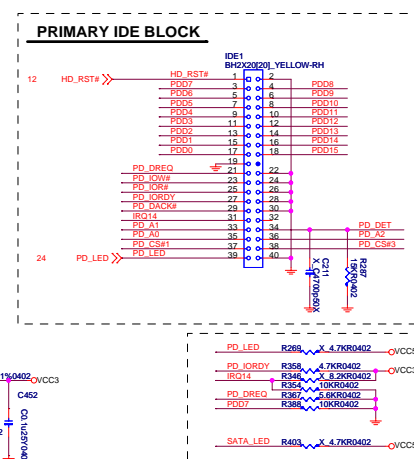
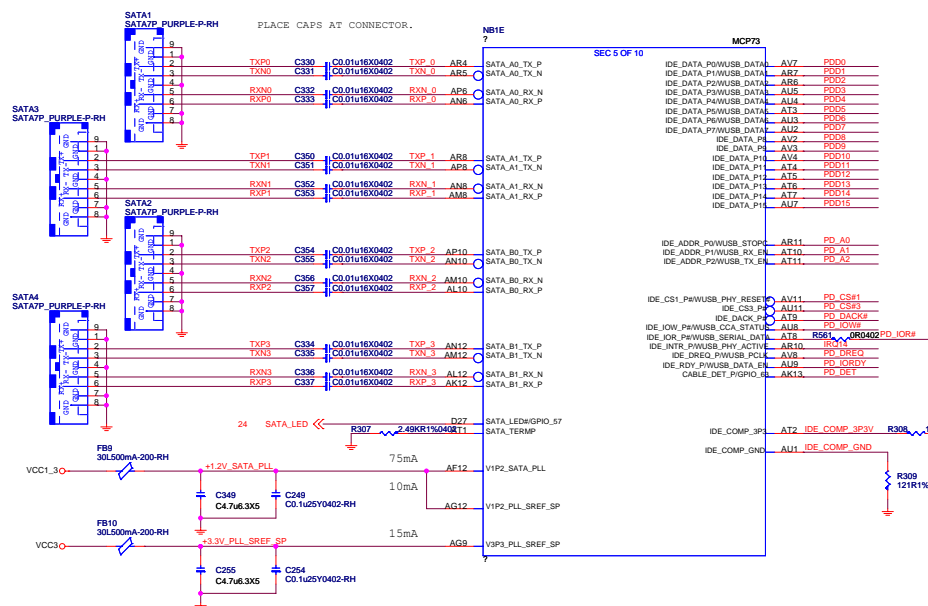


Demo Board with 0.1u X5, 1uX3, 10uX3 for Single Channel
Dual Channel Must x2





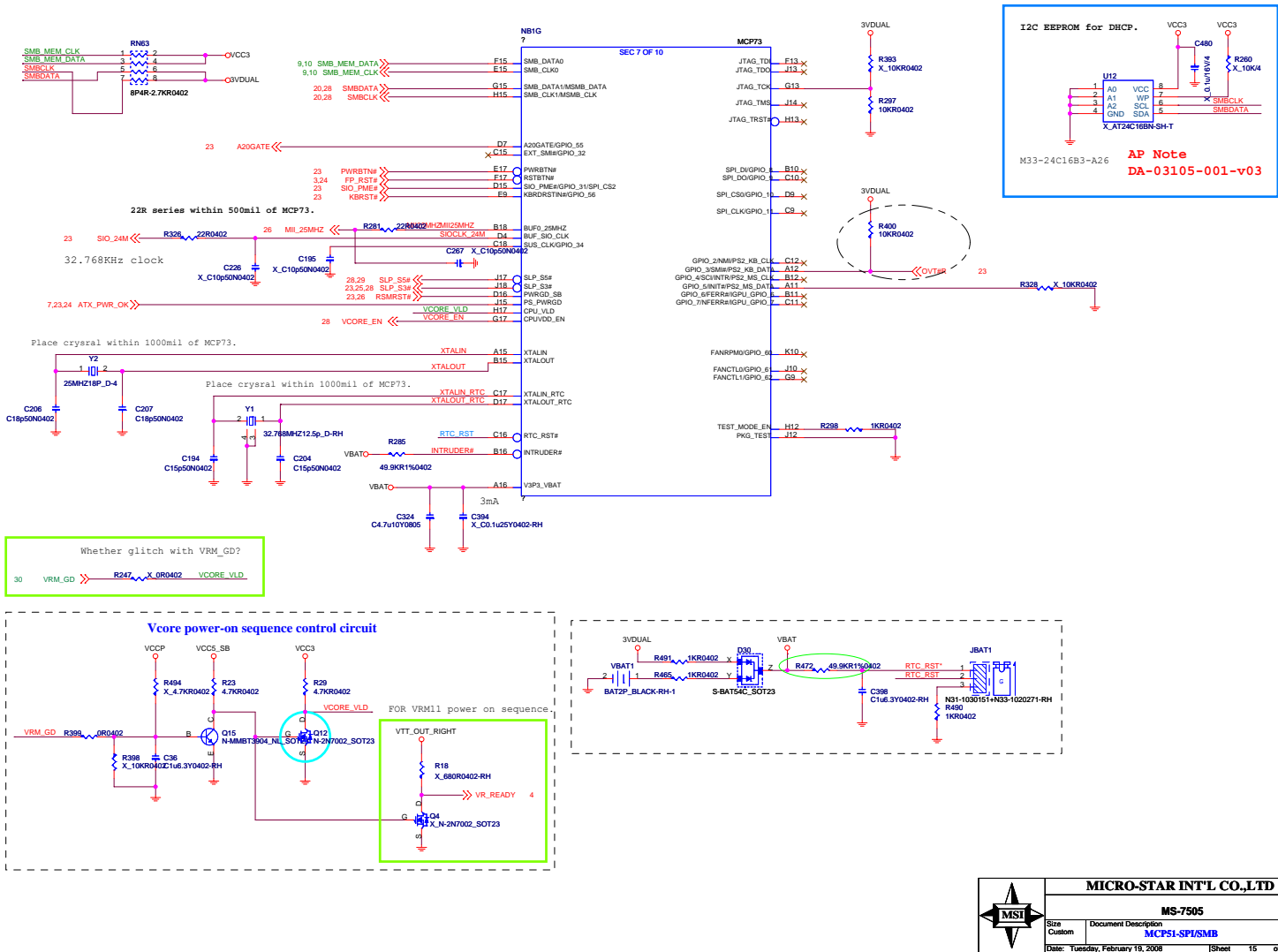
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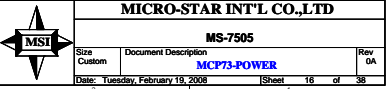


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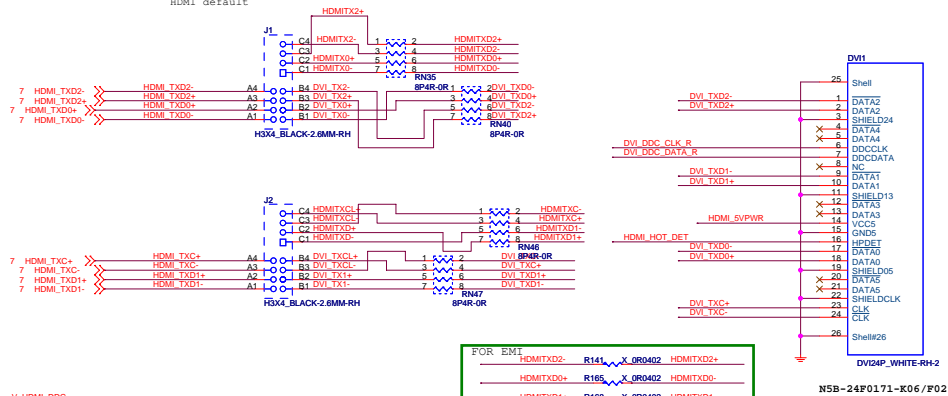
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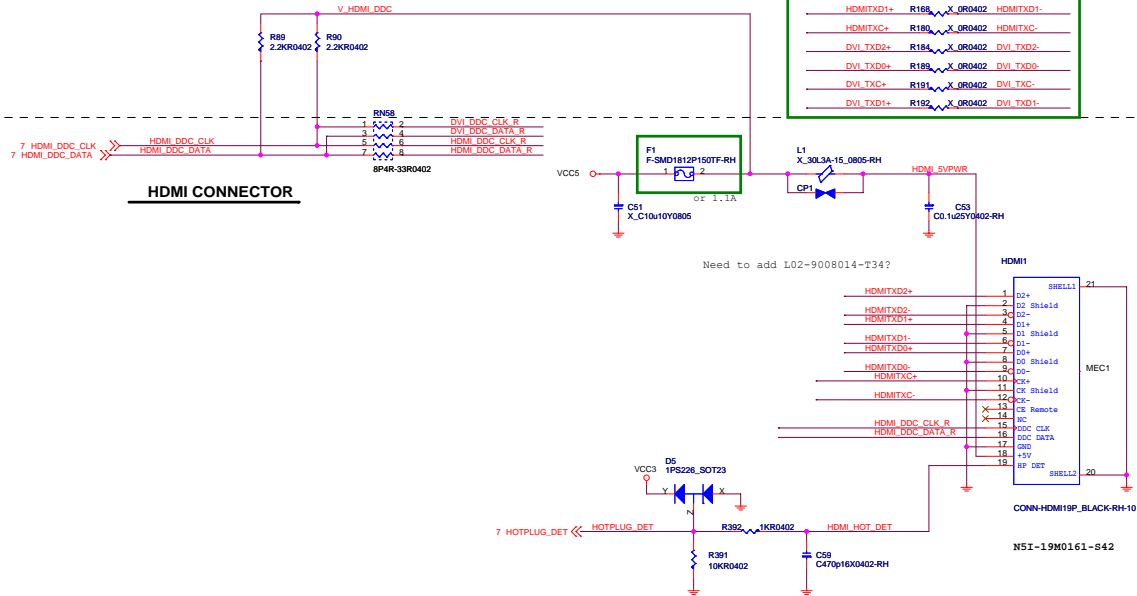


DVI CONNECTOR

HDMI default

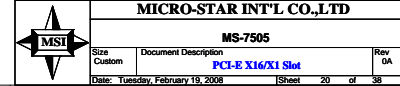
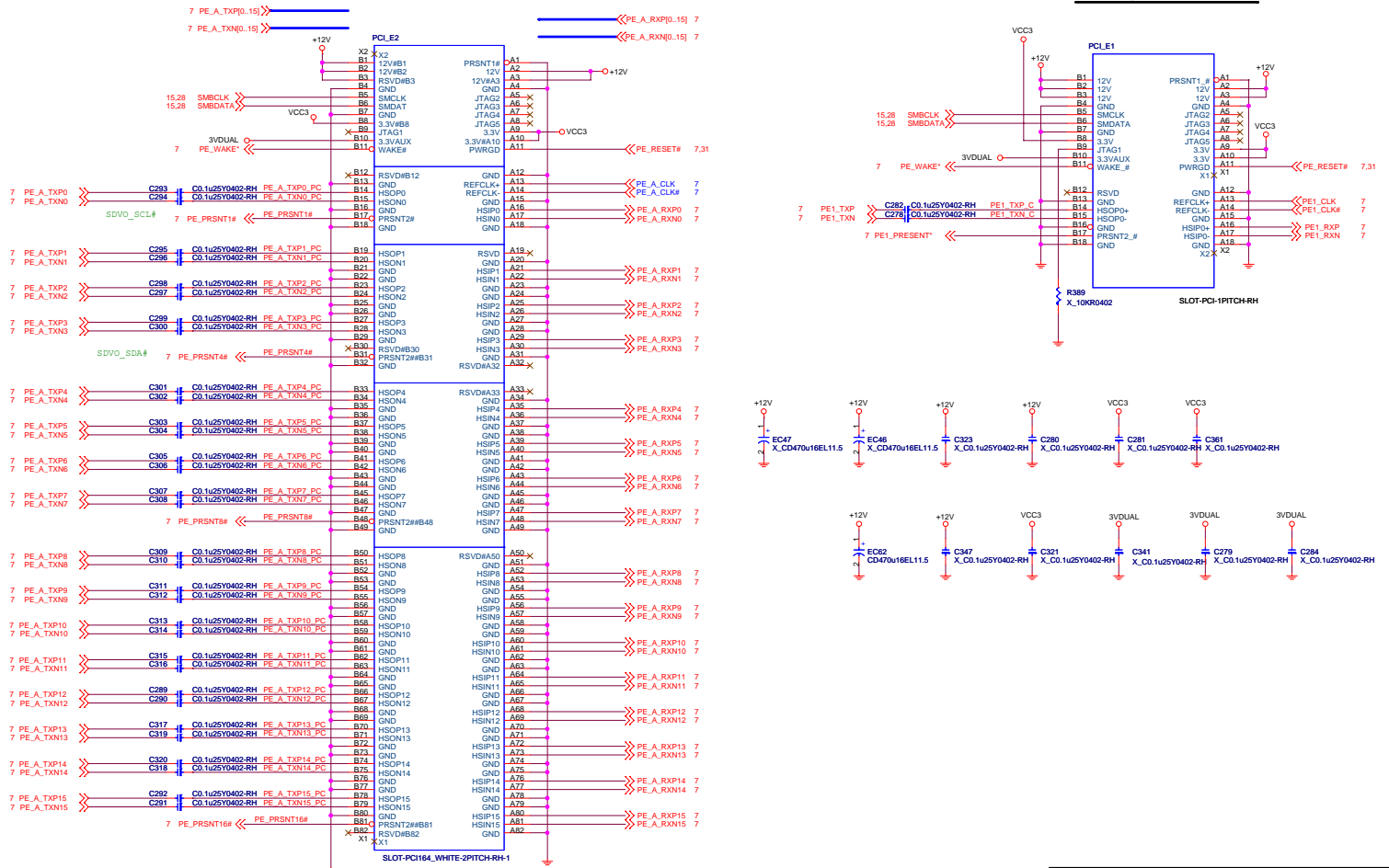
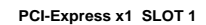


HDMI CONNECTOR

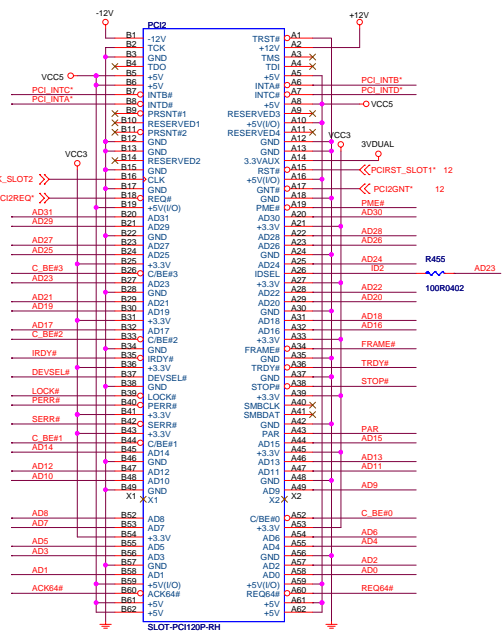


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PCI-Express X16 Primary Slot X16/X8



PCI SLOT 2 (PCI VER: 2.2 COMPLY)



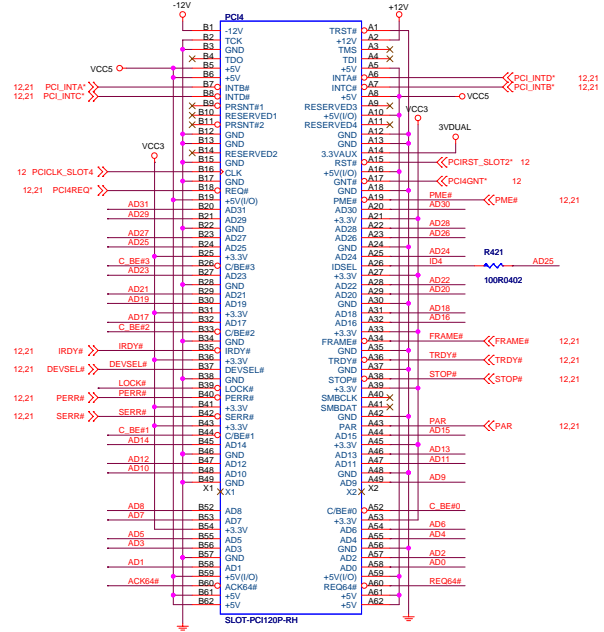
```
IDSEL = AD23
MASTER = PCI2REQ*
PCI2GNT*
```

The figure shows three separate circuit diagrams, each representing a different power supply configuration for the modules:


- Left Diagram:** A module labeled EC61 is connected to a VCC5 supply. The module's pin 1 is connected to VCC5 and pin 2 is connected to ground. The module is identified as X_CD470u16EL11.5.
- Middle Diagram:** A module labeled EC60 is connected to a VCC3 supply. The module's pin 1 is connected to VCC3 and pin 2 is connected to ground. The module is identified as CD470u16EL11.5.
- Right Diagram:** A module labeled EC52 is connected to a 3VDUAL supply. The module's pin 1 is connected to 3VDUAL and pin 2 is connected to ground. The module is identified as X_CD470u16EL11.5.



PCI SLOT 1 (PCI VER: 2.2 COMPLY)



```
IDSEL = AD25
MASTER = PCI4REQ*
PCI4GNT*
```

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Schematic diagram of the CPU VID reset circuit. The circuit includes the following components and connections:

- CPUs:** CPU_BSEL2, CPU_BSEL1, CPU_BSEL0.
- Resistors:**
 - RN64: 2MR0402
 - R200: 2MR0402
 - RN85: 2MR0402
 - R208: 2MR0402
- Capacitor:** C124: C1000p500X0402
- Other Labels:** 3VDUAL, CPU VID reset, VBAT, JC11, COPEN, H1X3M_BLACK-RH.

Connections:

- CPUs CPU_BSEL2, CPU_BSEL1, CPU_BSEL0 are connected to RN64.
- CPUs CPU_BSEL2, CPU_BSEL1, CPU_BSEL0 are connected to RN85.
- CPUs CPU_BSEL2, CPU_BSEL1, CPU_BSEL0 are connected to R200.
- R200 is connected to VBAT.
- VBAT is connected to R208.
- R208 is connected to JC11.
- JC11 is connected to COPEN.
- COPEN is connected to H1X3M_BLACK-RH.
- H1X3M_BLACK-RH is connected to C124.
- C124 is connected to CPU_BSEL2.
- CPUs CPU_BSEL2, CPU_BSEL1, CPU_BSEL0 are connected to RN20.
- RN20 is connected to V_FSB_VTT.
- CPUs CPU_BSEL2, CPU_BSEL1, CPU_BSEL0 are connected to X_BP4R-470R0402.

Pin #	Pin Name	Description
Pin 1	DTnR#	1-SPFI 0-SPFI
Pin 2	RTSn#	1-Fan 0-Fan
Pin 5	30UTB	1-SPFI 0-SPFI
Pin 121	DTnR#	1-Power 0-Power
Pin 122	RTSn#	1-6 Pin 0-VID1
Pin 124	30UTn	1-Conf# 0-Conf#

```

on

Backup BIOS (Default)
Primary BIOS
rol Mode : PWM Mode.(Default)
rol Mode : Linear Mode.
tion Disable. (Default)
tion Enable.

Fan speed as Tot duty(FW0) (Default)
Fan with Full speed. (FW00)

VIDIN and VIDOUT (Default)
T on 6 pins, VIDOUT Pin will be GPIO.

Register I/O Port is 18/1F.(Default)
Register I/O Port is 2E/2F.

```

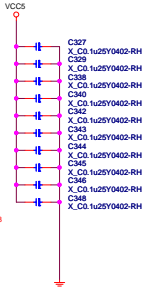
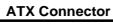
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3VDUAL VCC3
2
4
6 SERIRO
8 VCC5
12
14
H_BLACK-RH

Intel Front Panel



SYSTEM FAN



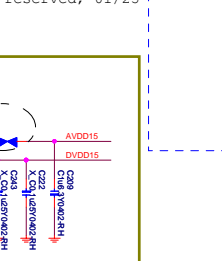
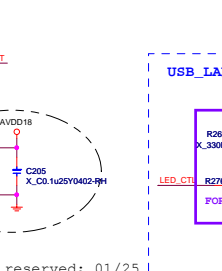
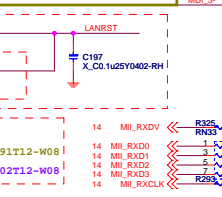
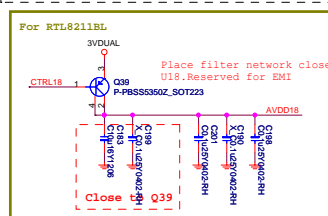
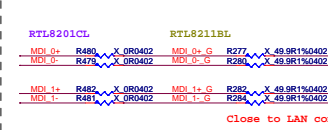
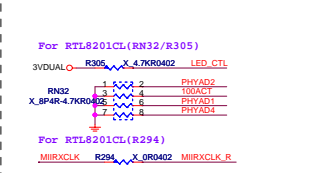
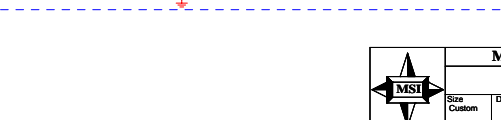
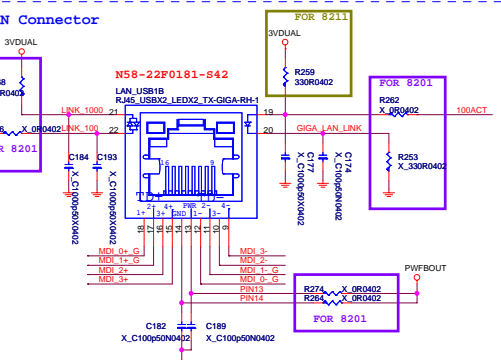
NB FAN







Reserve for NB_FAN, Near MCP73
MP Remove



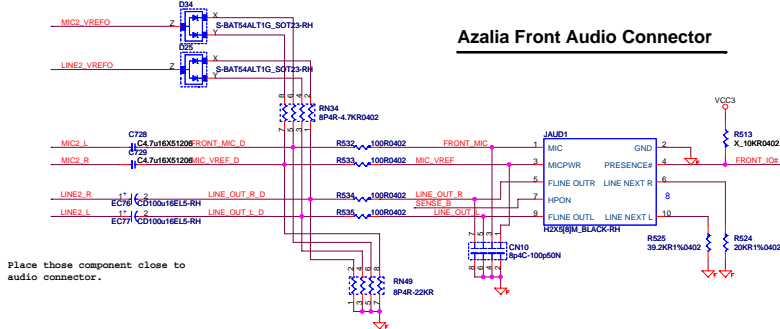
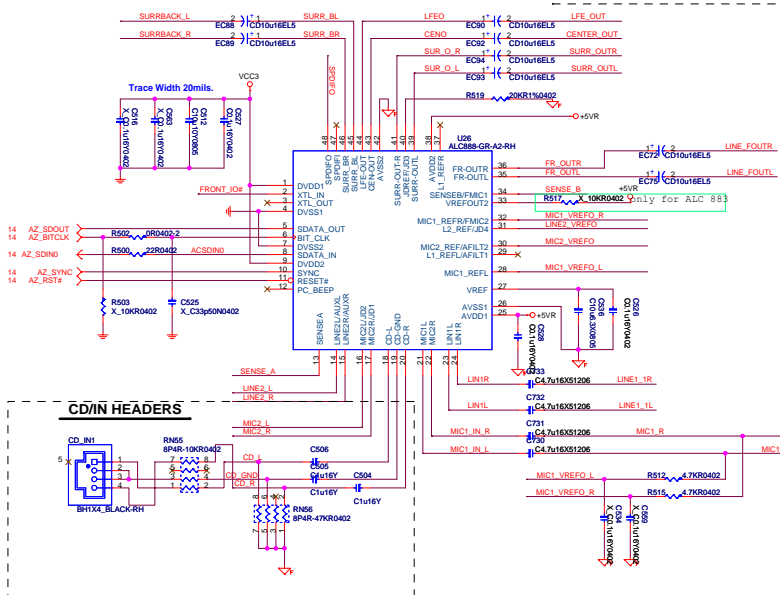
MICRO-STAR INT'L CO.,LTD			
MS-7505			
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U13				
MII_MDC	25	MDC	PWBOUT	32
MII_RXD0	26	MDC0	AVDD03	33
MII_TXD0	6	TXD0		
MII_RXD1	7	TXD1		
MII_TXD1	4	TXD2		
MII_RXD2	4	TXD2	AGND	28
MII_TXD2	5	TXEN	AGND	35
MII_RXEN	2	TXC		
MII_TXEN	3	RXD0		
MII_RXD3	22	RXD1		
MII_TXD3	21	RXD2		
MII_RXD4	20	RXD3		
MII_TXD4	19	RXD4		
MII_RXD5	18	RXD5		
MII_TXD5	17	RXD6		
MII_RXD6	16	RXD7		
MII_TXD6	15	RXD8		
MII_RXD7	14	RXD9		
MII_TXD7	13	RXD10		
MII_RXD8	12	RXD11		
MII_TXD8	11	RXD12		
MII_RXD9	10	RXD13		
MII_TXD9	9	RXD14		
MII_RXD10	8	RXD15		
MII_TXD10	7	RXD16		
MII_RXD11	6	RXD17		
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MII_RXD13	2	RXD21		
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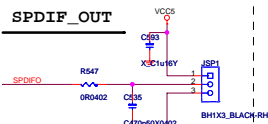
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Giga-Lan		10/100-Lan	
N58-22F0181-842		N58-22F0201-542	
Link Yellow		Link Yellow	
Active Blinking		Active Blinking	
1000 Orange		100 Green	
100 Green		10 None	
10 None			
19		19	
	Yellow		Yellow
21		21	
	Orange		
22		22	
	Green		Green

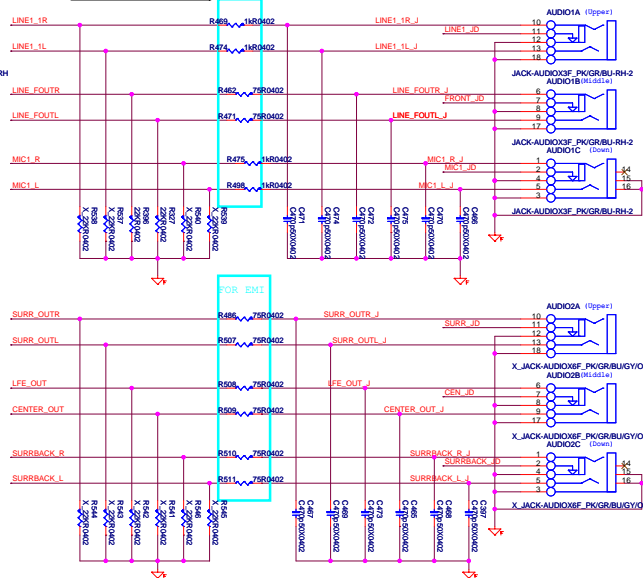
ALC888 CODEC



SPDIF_OUT



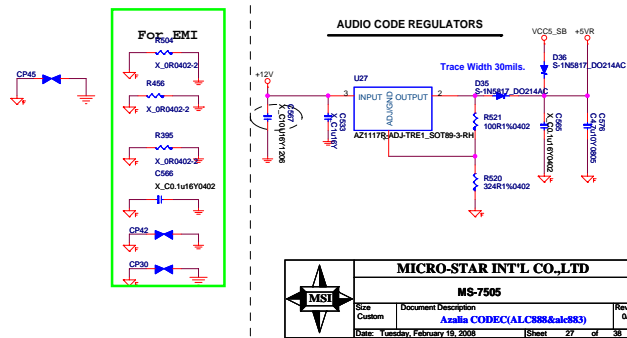
ALC883 JACK



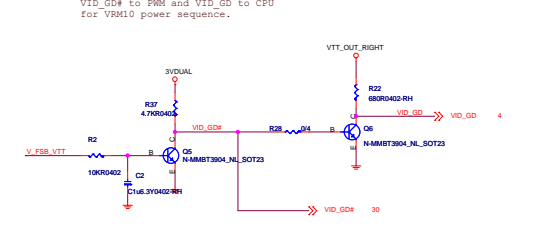
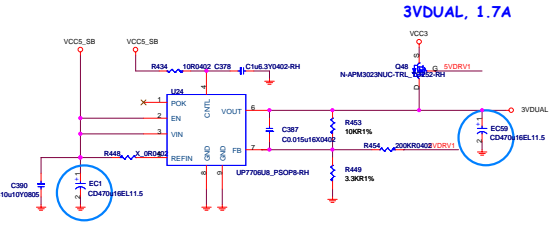
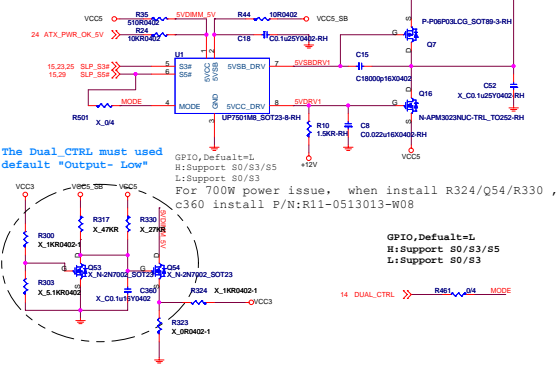
ALC883 JACK DETECT





AUDIO CODE REGULATORS



5VDIMM FOR DDR



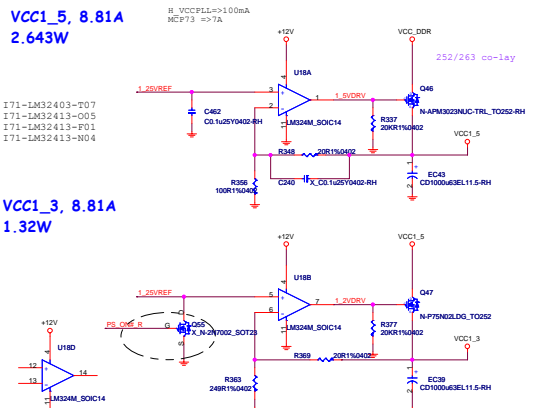
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DUAL_CTRL	X	X	0 1 1	0 1 1
SVSDRV1	1	0	1 0 0	1 0 0
SVDRV1	1	0	0 0 0	0 0 0
SVSDRV2	X	0	1 0 0	1 0 0
USB_MODE	X	1	X 1 0	X 1 0
SVDIMM	Y	Y	N Y Y	N Y Y
USB power	Y	Y	N 	N 

Reference Voltage

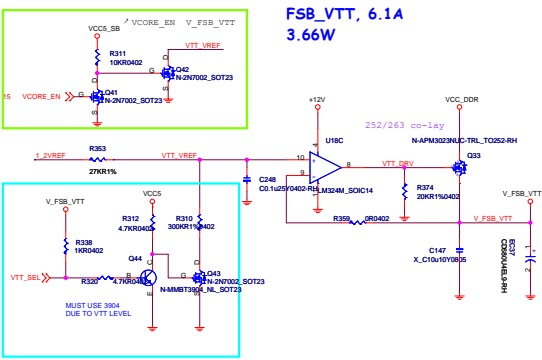
1_3VDUAL, 25mA

[illegible]

VCC1_5, 8.81A
2.643W



VCC1_3, 8.81A
1.32W



VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

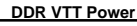
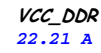


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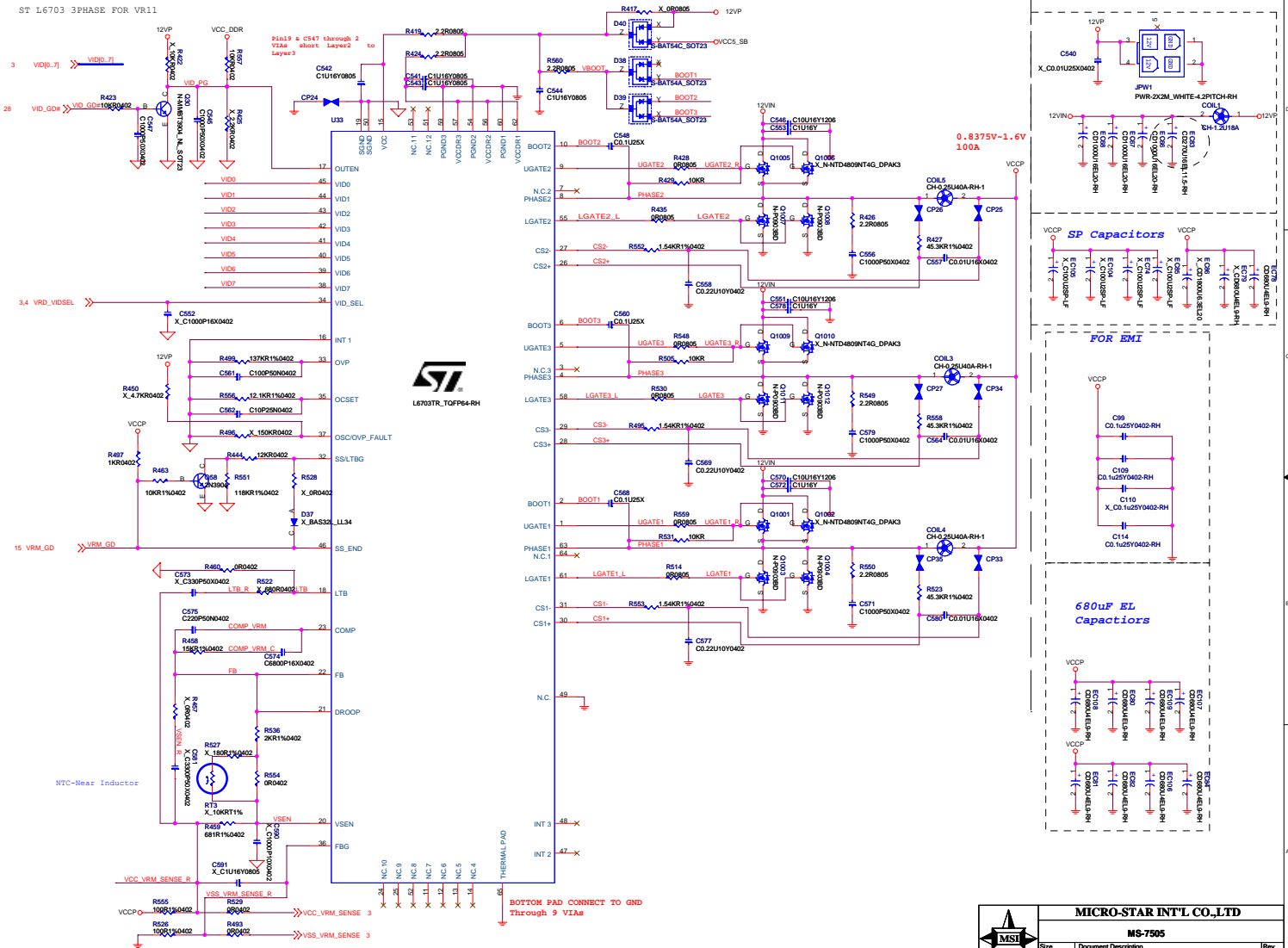
Custom	ACPI Controller UPI	0A
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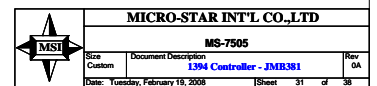
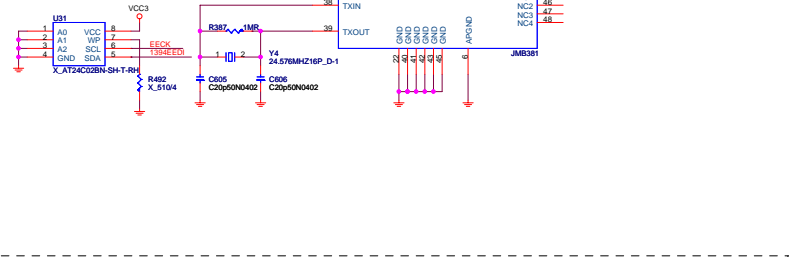
Date: Tuesday, February 19, 2008 Great 20 00 30

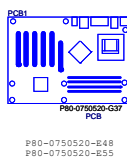
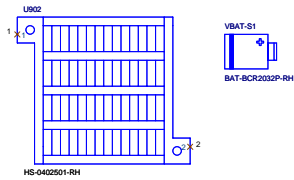
$$I_{ripple} = 22.21 \times 0.6 \times 0.8 / 1 = 10.66A$$
$$2.35 \times 3 \times 1.7 = 11.985A > 10.08A$$


To CPU Copper trace width > 200mils





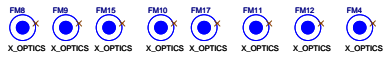




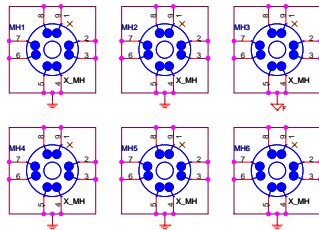
Optics Orientation Holes (F_PAD_M100)



Optics Orientation Holes (F_PAD_M120)



Mounting Holes



Simulation



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Custom	MANUAL PARTS		
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